The Importance of Microwave Approach for High Frequency MOS Analog Designers

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***Abstract*— Today analog products reach X and upper bands and integrated-circuit designers face new typical radio-frequency problems, especially when considering passive components. This paper choose to focus on inductor design and layout. After studying different kinds of layout, it is pointed out that the classical integrated solution cannot always meets circuit requirements and industrial constraints. Discussion about the alternative hyper frequency choice is done and a design flow method is provided.**

***Index Terms*—coplanar waveguide, inductors, CPW, SOS**

I. Introduction

With the increasing need for low-cost, high-power and large bandwidth products for the multimedia mobile systems, the challenges in the area of radio frequency (RF) and mixed-signal System-On-Chip (SOC) will become important. GaAs ICs and SiGe ICs are classically used for high power and high frequency operations, but silicon ones will enable lower cost solutions for many reasons. The first on eis due to the fact that the cost of digital tehcnologies is going lower and lower because of the growth of the personal electronic especially thanks to computers. Then, even if considerations were made on flip chip attachment to package and embedded passives on it, the traditional solutions of low inductance and high-density packages like fine pitch ball grid array (FBGA) or chip scale packaging (CSP) are always linked to a higher cost than mono-chip systems. The solution for the future is to use the same technology for both digital processing and analog part. For analog people, the challenge is to find new RF structures in digital CMOS technologies or to generalize technology transpositions. The study of those classical RF structures shows that the main point is that most of high frequency structures use self inductors either for filter design, DC polarization or resonator realization. In many designs, since active components have little gain, passive ones must have the lowest loss. The purpose of this work is thus to take a look at the realization of a particular on-chip printed inductor in a SOS (Silicon On Sapphire) technology and to introduce a global reflection about the meeting of two high frequency design approaches : the analog and the microwave ones. First, classical models of both domains of integrated self-inductors will be analyzed. Then, an actual design using classical analog approach will be computed. Third performances will be discussed and limits of printed spiral inductors will be pointed out. The microwave aspect will be investigated and conclusion on our particular case given.

II. Integrated inductors state of art

A. The microwave designer point of view

Historically, the hyper frequency approach, because of the particular die of GaAs substrate, used to realize passive components by layouting microstrips (fig. 1-(a)). With new technologies, new structures appear and microstrip can be generalized to striplines in fig. 1-(d) when using a top shield. In cases where ground plane is not available, coplanar waveguides (CPW) (fig. 1-(b)) and slotlines (fig. 1-(c)) are useful. And of course studies were made on those latter two structures when a ground shield exists and such solutions can also always be used. If analog people tend to see each type of line as a particular layout of self inductor with less than one turn, the traditional point of view, coming from physical cables, uses the different approach and calculus method of waveguides.

First, the well known telegrapher formula must be used and leads to the line impedance :

$$Z(l) = Z_c \frac{Z_R + jZ_c tan(\beta l)}{Z_c + jZ_R tan(\beta l)} \tag{1}$$

depending on l, the length of the line, Z_R, the charge impedance and $\beta = \omega/v$ with $v = c/\sqrt{\epsilon_{re}}$ the actual speed.

Z_c is the characteristic impedance of the line that must be considered. If we use an SOS technology without ground plane, the CPW solution of fig. 1-(b) is perfectly adapted and Z_c can be written, even for X band, as ([1] issued from the quasi-static model of [2]) :

$$Z_c = \frac{30\pi}{\sqrt{\epsilon_{re}}} \frac{K'(k)}{K(k)} \tag{2}$$

where

$$k = \frac{w}{w + 2s} \tag{3}$$

and $K(k)$ is the complete elliptic integral of the first kind. The literature with [3] gives an accurate expression of the ratio $K'(k)/K(k)$ that is :

$$\frac{K(k)}{K'(k)} = \frac{1}{\pi} ln\Big(2\frac{1+\sqrt{k}}{1-\sqrt{k}}\Big) \tag{4}$$

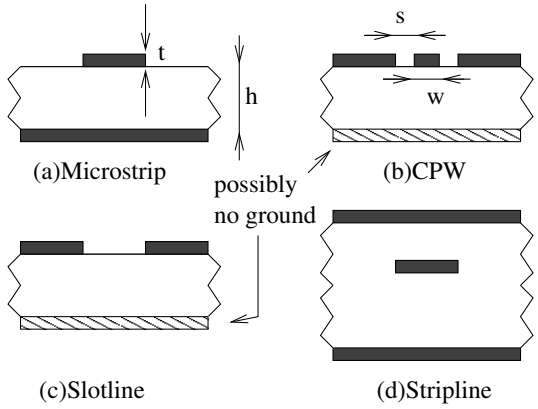

Fig. 1. Different kinds of striplines

for $\sqrt{2} < k \leq 1$ and

$$\frac{K(k)}{K'(k)} = \frac{\pi}{ln(2\frac{1+\sqrt{k'}}{1-\sqrt{k'}})} \tag{5}$$

for $0 \leq k \leq \sqrt{2}$ with $k' = \sqrt{1-k^2}$
Finally, results from Bahl in [4] give :

$$\epsilon_{re} = \frac{\epsilon_r + 1}{2} \tag{6}$$

when there is either no or far away ground plane.

B. The analog designer point of view

From the historical point of view of analog design, the systematic approach of the physical study of inductors gives a frequency response that shows three workings zones : as an inductor, a resistor and a capacitor, depending on frequency. Thus, the classical model of fig. 2 can be derived (see [5], [6], [7] and [8]). In the case of on-chip printed inductors, we cannot neglect losses into substrate that are modeled by grounded coupling capacitors in series with resistors that stand for the resistivity of the substrate (fig. 3 from [9]). Note that this last effect is power-consuming and thus must be avoided either with a perfect insulator (and in this case the return path is a grounded shield under substrate) or with a perfect conductor that is, for example a grounded shield over the substrate ([6]). Capacitors are another problem that can be deleted while removing return paths, as, for example in an SOS technology with no ground layer under the substrate. And in this particular example, the schematic of fig. 2 is still usable. Thus, the main point remain the inductance. In the twenties, Wheeler computed a formula ([10]) that was update in [5] in order to match to our nowadays requirements on MOS integrated technologies :

$$L_{mw} = K_1 \mu_0 \frac{n^2 d_{avg}}{1 + K_2 \rho} \tag{7}$$

with

n : number of turns
w : track width
s : gap between tracks
$\rho = \frac{d_{out} - d_{in}}{d_{out} + d_{in}}$: density filling

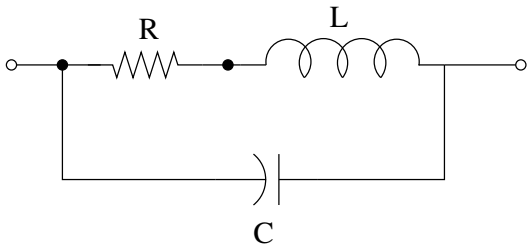

Fig. 2. Natural inductor model

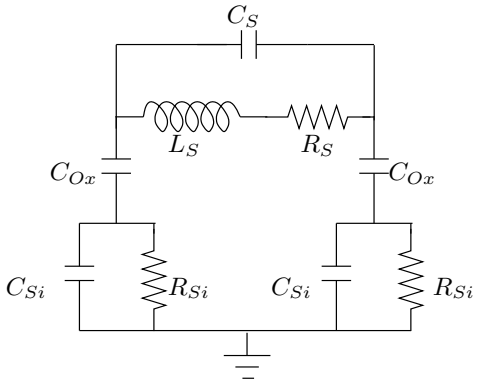

Fig. 3. Lumped inductor model

$d_{avg} = 1/2(d_{out} + d_{in})$: mean diameter
d_{in} and d_{out} : internal and external diameters of the inductors
K_1 and K_2 : shape coefficients. If we want to study the square case, empirical results given in [5] are $K_1 = 2.34$ and $K_2 = 2.75$.

This formula is claimed to have the same accuracy than the one computed by electromagnetic calculation or statistical model extraction. But its main advantage comes from the fact that it allows formal calculus. And since for very high frequency, where there is no negligible length, only the experiment can give true results, we will use this modified Wheeler formula for this theoretical work.

However, we cannot neglect the other important value that is to be specified when an inductor is needed : its quality factor Q that is the ratio between the stocked and the lost energy ([11]). With our inductor model fig. 3, we can write with a good approximation for first order calculus that :

$$Q = \frac{\omega L}{R_s} \tag{8}$$

Finally, we must note that models from fig. 2 or 3 are not linked to the way L is calculated. Thus (8) can also be applied in case of microstrips described in the previous section.

III. DESIGN AND LIMITS OF AN ANALOG INDUCTOR ON AN SOS$0.5\mu m$ TECHNOLOGY

Let us now assume that we want to layout an inductor defined by $L = 200pH$ and $Q = 20$ for a use at $f = 10GHz$

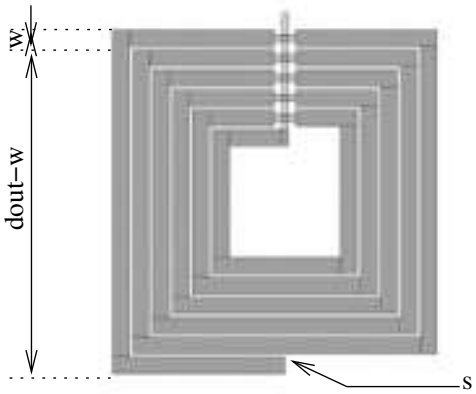

Fig. 4. Square integrated inductor

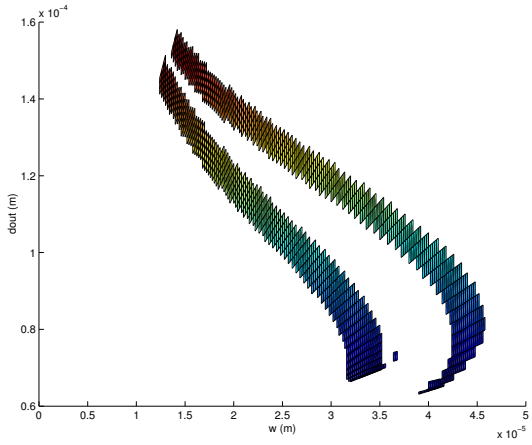

Fig. 5. d_{out} versus w with s as a parameter for square inductors

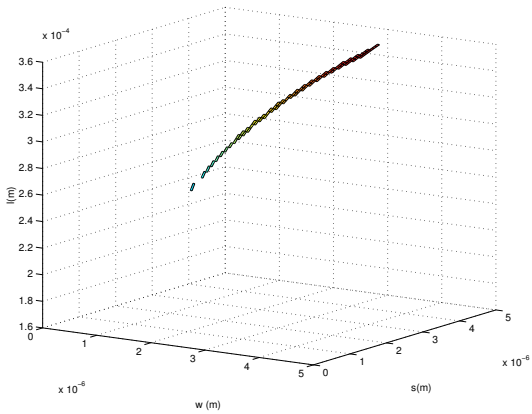

Fig. 6. l versus w and s for CPW

on the SOS $0.5\mu m$ technology of section II on which conductivity $\sigma = 3.57\,10^7 S/m$ and metal thickness $t = 3.1\mu m$. If we want to use the classical analog square approach,we first see that the main point in (8) is that we need R_s. The easiest way to have it is to use the direct formula that gives :

$$R_s(l) = \frac{l}{\sigma w t} \tag{9}$$

where σ is the conductivity of the metal layer for a given section wt. Then we must remember that the main point in integrated inductor design is the area : from an industrial point of view, interest of inductors is linked to their quality to cost ratio. Thus let us assume that our design criterion is d_{out}. Now, for the square inductors of fig. 4, we can write that the k^{th} turn from outside has a diameter $d(k) = dout - 2k(w+s)$. This leads to both

$$d_{in} = d_{out} - 2(n-1)(w+s) \tag{10}$$

and

$$l = 4\Big[n(dout - w) - 2(w+s)\frac{n(n-1)}{2}\Big] \tag{11}$$

where l is the total length of the path, the latter equation coming from a recursive formula based on the fact that one turn length is $4(d(k) - w)$ (fig. 4), neglecting input and output path effects. Thus, (7) can also be written as :

$$L_{mw} = \frac{K_1 \mu_0 n^2 [d_{out} - (n-1)(w+s)]}{1 + K_2 \frac{(n-1)(w+s)}{d_{out} - (n-1)(w+s)}} \tag{12}$$

And (11) can be solved in :

$$n = \frac{1}{2(w+s)}\Big[d_{out} + s \pm \sqrt{(d_{out}+s)^2 - l(w+s)}\Big] \tag{13}$$

Fig. 5 is the graphical solution for system (12) and (13) in d_{out} for s and w stick to design rules of most of technologies (between $1\mu m$ and $50\mu m$). The only solutions appear for s between 1 and $2\mu m$. Thus it shows that our given inductor can not be layouted since those values are not allowed by many design rules. Moreover, it seems that the most realistic values (for $w < 15\mu m$) gives a minimum die area as a square of $150\mu m$x$150\mu m$ which is very expensive if we need a full differential mono-chip integrated front-end with many inductors.

IV. Discussion around solutions and needs

As shown in previous section, layout of low-L high-Q inductors using the classical square spirals under industry conditions cannot be done. On an SOS$0.5\mu m$ technology, as it is explained in section II, another solution for layouting self inductors is to use coplanar waveguides (CPW) under the hypothesis that there is no ground plane under the sapphire substrate ($\epsilon_r = 10.5$). Using (1) with $Z_R = 0$, we have $Z(l) = Z_c \beta l$ if the frequency is high enough to consider that $\beta l \ll 1$. Thus, with (2), we have the following formula for l depending on L :

$$l = \frac{cLK(k)}{30\pi K'(k)} \tag{14}$$

Trying to make an inductor of 200pH is feasible and leads using (14) with (4) or (5) to fig. 6, 7 and 8 to $w = 1\mu m$, $s = 4\mu m$ and l about $260\mu m$ which use about $260 * (1 + 4 * 2) * 10 = 23400\mu m^2$ (taken into account infinite border planes). In this case the occupied area is similar to our previous design using classical square inductors, but here, we perfectly meet design requirements and technologies design

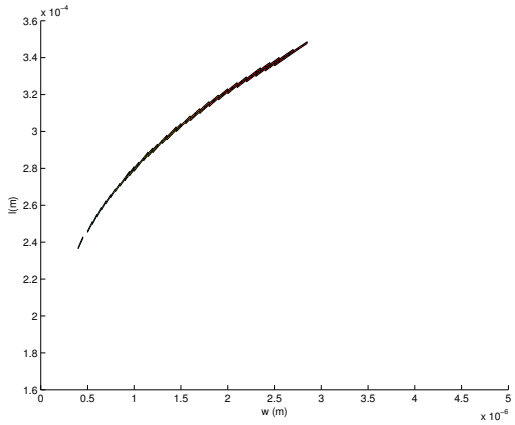

Fig. 7. l versus w for CPW (fig. 6 projection)

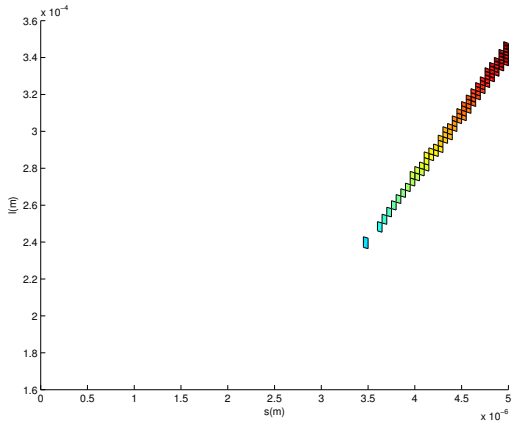

Fig. 8. l versus s for CPW (fig. 6 projection)

rules. Finally, what was shown here is that the analog RF designer must always think to the microstrip solution when the layout of inductor is needed. The method proposed here consists in starting the layout by solving (12) and (13) first. If the result in d_{out} does not match the desired industrial criterion, (14) must be computed in order to compare solutions. Then, the best one from the occupied area point of view has to be chosen. Thus it seems useful for future work to have a direct computable criterion. This will be the topic of another paper.

V. Conclusion

In this paper, we have pointed out an issue that can be encountered by analog designers when they are trying to layout low-L, high-Q inductors. The problem has clearly been shown with characteristics of an SOS$0.5\mu m$ technology : from an industrial point of view, in which cost is linked to chip area, some low inductance high Q inductors cannot be layouted using classical printed spirals. The method to detect such a problem early in the design process has been shown. Then, the solution of microstrip and especially coplanar waveguide has be proven to have better performances in some situations, and general equations for practical applications have been given.

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