CRITERION OF DESIGN FOR SMALL VALUE INTEGRATED SELF-INDUCTORS

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ABSTRACT

Facing the increase in frequency of use of analog products, integrated-circuits designers reach X or upper band and their own problems, especially in the case of passive components. This paper focus on inductor design and layout, opposing classical analog integrated inductors and hyper frequency lines. After studying separately each solution and pointing out their limits on an actual SOS $0.5\mu m$ case, a methodology to solve this issue is exposed and a choice criterion is supplied.

1. INTRODUCTION

The challenges in the area of radio frequency (RF) and mixed-signal System-On-Chip (SOC) will become important as low-cost mobile and high bandwidth products derive across several market segments. The increasing performances of silicon ICs will enable lower cost solutions in the frequency domain below 10 GHz. GaAs ICs and SiGe ICs are now used for higher frequency or power applications. Signal integrity and cost issues become dominant. Considerations were made on flip chip attachment to package and embedded passives on this package. But the traditional solution of low inductance and high-density packages like fine pitch ball grid array (FBGA) or chip scale packaging (CSP) are always linked to a higher cost than mono-chip systems. The solution for the future is to use the same technology for both digital processing and analog part. This can only be done by parallelizing these two types of research. In the digital electronic and signal processing domain, higher speed analog to digital converters (ADC) are required, joined to harder data recovering algorithms. For analog people, the challenge is to find new RF structures in submicronic digital CMOS technologies or to generalize technology transpositions. The main point with such an objective appears instantly : most of high frequency structures use self inductors either for filter design, DC polarization or resonator realization. The purpose of this work is thus to take a look at the evolution and perception of on-chip printed inductors in order to show limits of this solution on MOS (and especially SOS - Silicon On Sapphire) technologies and to offer method of design with a choice criterion between different structures. First, classical models of printed self-inductors will be analyzed in order to understand which effects are neglected at each step. Then, the main other solution that is already classically used in GaAs technology will be investigated : this is the one that use microstrip. Third limits of printed spiral inductors will be pointed out by using numerical values of an SOS technology. Finally a general design method will be exposed, joined to a choice criterion.

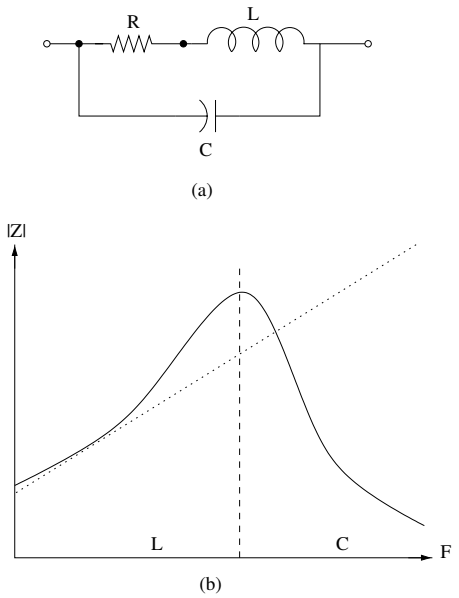

Figure 1. (a) Natural inductor model and (b) Inductors frequency behavior

2. PRINTED SPIRAL INDUCTOR SIMPLE ACCURATE EXPRESSION

When studying the physic of inductors, especially when having a look at the frequency behavior (fig. 1-(b)), the classical model of fig. 1-(a) can be extracted (see [1], [2], [3] and [4]). In the case of on-chip printed inductors, we cannot neglect losses into substrate that are modeled by grounded coupling capacitors in series with resistors that stand for the resistivity of the substrate (fig. 2 from [5]). Note that this last effect is power-consuming and thus must be avoided either with a perfect insulator (and in this case the return path is a grounded shield under substrate) or with a perfect conductor that is, for example a grounded shield over the substrate ([2]). Capacitors

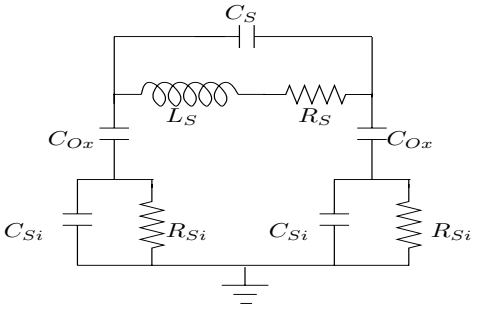

Figure 2. Lumped inductor model

can only be deleted by having no return path, as, for example in an SOS technology with no ground layer under the substrate. Concerning model in the printed case, first work was done by Wheeler in the twenties ([6]). Updating his results for nowadays MOS integrated technologies, [1] gives us the following formula, that is claimed to be true at three percent compared to physical electromagnetic simulators :

$$L_{mw} = K_1 \mu_0 \frac{n^2 d_{avg}}{1 + K_2 \rho} \tag{1}$$

with

n : number of turns
w : track width
s : gap between tracks
$\rho = \frac{d_{out} - d_{in}}{d_{out} + d_{in}}$: density filling
$d_{avg} = 1/2(d_{out} + d_{in})$: mean diameter
d_{in} and d_{out} : internal and external diameters of the inductors
K_1 and K_2 : shape coefficients

Table 1. Shape coefficients for the modified Wheeler formula

Shape	K_1	K_2
Square	2.34	2.75
Hexagonal	2.33	3.82
Octagonal	2.25	3.55

Some other formulas based either on electromagnetic calculation or on statistical model extraction are given, but since results have the same accuracy, we will use the modified Wheeler equation for further works. The other important value that is to be specified when an inductor is needed is its quality factor Q that is the ratio between the stocked and the lost energy ([7]). With our inductor model fig. 2, we can write that :

$$Q = \frac{\omega L}{R_s} \tag{2}$$

3. MICROSTRIP AND COPLANAR WAVEGUIDE

Coming from the GaAs hyper frequency technologies, microstrip is another way of doing components, named distributed ones. They can be of a lot of types, from actual microstrips (fig. 3-(a)) to striplines (fig. 3-(d)) passing by coplanar waveguides (CPW) (fig. 3-(b)) and slotlines (fig. 3-(c)) the latter two with or without ground. If one can see each type of line as a particular layout of self inductor with less than one turn, the traditional point of view, coming from physical cable, tends to use different approach and calculus method. First of all, let us consider the characteristic impedance of the line of fig. 3-(b) that is perfectly usable with SOS technology and write, even for X band ([8] issued from the quasi-static model of [9]) :

$$Z_c = \frac{30\pi}{\sqrt{\epsilon_{re}}} \frac{K'(k)}{K(k)} \tag{3}$$

where

$$k = \frac{w}{w + 2s} \tag{4}$$

and $K(k)$ is the complete elliptic integral of the first kind. The literature with [10] gives an accurate expression of the ratio $K'(k)/K(k)$ that is :

$$\frac{K(k)}{K'(k)} = \frac{1}{\pi} ln(2 \frac{1 + \sqrt{k}}{1 - \sqrt{k}}) \tag{5}$$

for $\sqrt{2} < k \leq 1$

$$\frac{K(k)}{K'(k)} = \frac{\pi}{ln(2 \frac{1+\sqrt{k'}}{1-\sqrt{k'}})} \tag{6}$$

for $0 \leq k \leq \sqrt{2}$ and $k' = \sqrt{1 - k^2}$
Finally, results from Bahl in [11] give :

$$\epsilon_{re} = \frac{\epsilon_r + 1}{2} \tag{7}$$

when there is either no or far away ground plane. The next step is to remember that for any lossless transmission lines the telegrapher formula leads to (8).

$$Z(l) = Z_c \frac{Z_R + j Z_c tan(\beta l)}{Z_c + j Z_R tan(\beta l)} \tag{8}$$

where l is the length of the line, Z_R is the charge impedance and $\beta = \omega / v$ with $v = c/\sqrt{\epsilon_{re}}$ the actual speed. Eventually, as in the case of inductors, the definition of Q in (2) is still valid.

4. ANALYSIS OF PERFORMANCES ON AN SOS$0.5\mu M$ TECHNOLOGY

The main point in (2) is that we need R_s. The easiest way to have it is to use the direct formula that gives :

$$R_s(l) = \frac{l}{\sigma} \tag{9}$$

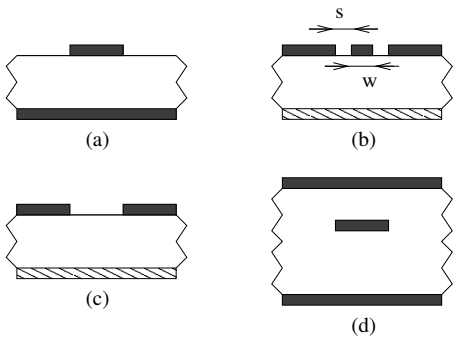

Figure 3. Different kinds of striplines

where σ is the conductivity of the metal layer for a given section. Then one must be aware that the main point in integrated inductor design is the area : from an industrial point of view, interest of inductors is linked to their quality to cost ratio. Thus let us assume that we have a fixed area, that is d_{out} is a fixed value. Moreover, for the square inductors of fig. 4, we can write that the k^{th} turn from outside has a diameter $d(k) = dout - 2k(w+s)$. This leads to both

$$d_{in} = d_{out} - 2(n-1)(w+s) \tag{10}$$

and

$$l = 4\Big(n(dout - w) - 2(w+s)\frac{n(n-1)}{2}\Big) \tag{11}$$

where l is the total length of the path, the latter equation coming from a recursive formula based on the fact that one turn length is $4(d(k)-w)$ (fig. 4), neglecting input and output path effects. Thus, (1) can also be written as :

$$L_{mw} = \frac{K_1 \mu_0 n^2 [d_{out} - (n-1)(w+s)]}{1 + K_2 \frac{(n-1)(w+s)}{d_{out}-(n-1)(w+s)}} \tag{12}$$

And (11) can be solved in :

$$n = \frac{1}{2(w+s)}\Big[d_{out} + s \pm \sqrt{(d_{out}+s)^2 - l(w+s)}\Big] \tag{13}$$

Fig. 5 is the graphical solution for system (12) and (13) in l (that is equivalent to R and thus Q) for L from 100pH to about 1nH, $w = 5\mu m$ and s between $1\mu m$ and $50\mu m$ which are classical values on CMOS substrate. Fig. 6 shows that for a given d_{out} the quality factor cannot be extended to usable values for extremely low inductance L or at high frequencies, where s must be large enough to minimize C_s and to make the inductor stay in the "L area" of fig. 1. On an SOS$0.5\mu m$ technology, as it is explained in previous section, another solution for layouting self inductors is to use coplanar waveguides (CPW) under the hypothesis that there is no ground plane under the sapphire substrate ($\epsilon_r = 10.5$). Using (8) with $w = 5\mu m$, $s = 30\mu m$ and $Z_R = 0$, we have

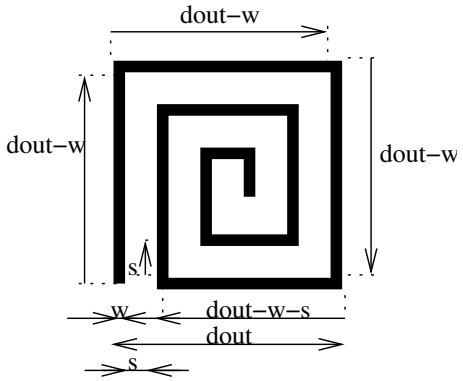

Figure 4. Square integrated inductor

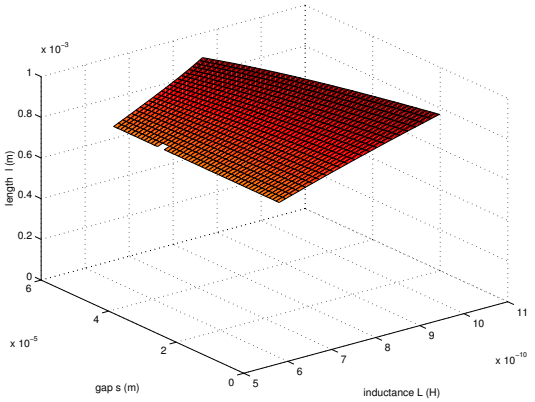

Figure 5. l versus L and s for square inductors

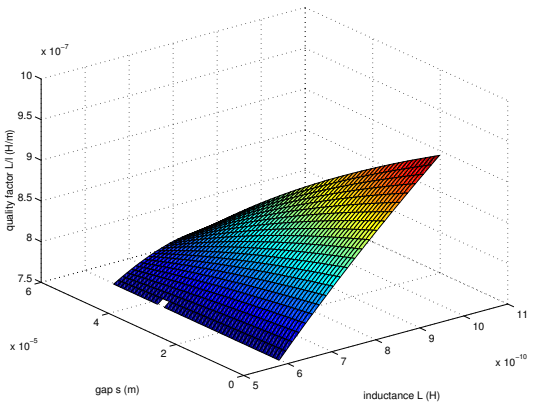

Figure 6. L/l versus L and s for square inductors

$Z(l) = Z_c \beta l$ if the frequency is high enough to consider that $\beta l \ll 1$. Thus, we have the following formula for l depending on L :

$$l = \frac{cL}{Z_c \sqrt{\epsilon_{re}}} \tag{14}$$

Trying to make an inductor of 200pH is feasible and leads to $l = 256\mu m$ which use less area than classical square inductors of higher values.

5. DISCUSSION ABOUT DESIGN METHOD AND CHOICE CRITERION

As shown in previous section, layout of low value inductors using the classical square spirals under industry conditions leads to low Q or cannot be done. The alternative way consists in layouting a kind of striplines depending on the technology. The choice criterion (CC) consists in computing :

$$CC = \frac{l_{for\ spiral\ inductor}}{l_{for\ CPW}} \tag{15}$$

using (12), (13), (3) and (14). In the case of $CC \leq 1$ the analog solution must be used and a square inductor layouted. Otherwise, microwave line has to be drawn. The main point here is the choice of which values have to be fixed and which must be a variable. From an integrated-circuit industry point of view, external physical dimensions must be chosen prior to any calculus. Note that it implies, in the CPW case, the maximum value of $w + s$ in order to stay under infinite border ground plane hypothesis (we should have $(w + s) \ll d_{out}$). s is generally fixed in order to have a resonant frequency higher than the one of use while design rules are checked. Then, it depends on what is needed : we can either fix L and search for n or do the opposite. For example, let us choose typical values of $s = 10\mu m$ and $w = 5\mu m$ for $d_{out} = 200\mu m$. Computing CC gives fig. 7. This result shows first that value under 500nH can't be reached with square spiral under that condition, and thus CPW is the best solution, whereas for higher values, the classical printed spiral inductor gives a higher Q.

6. CONCLUSION

In this paper, we have pointed out an issue that can occur when trying to layout printed integrated inductors. The problem has clearly been shown with characteristics of an SOS$0.5\mu m$ technology : in an industrial way, in which each area has high cost, some low inductance high Q inductors cannot be layouted using classical printed spirals. Thus a method has been proposed in order to detect such a problem early in the design process and an alternative solution with formulas for performances comparison was given.

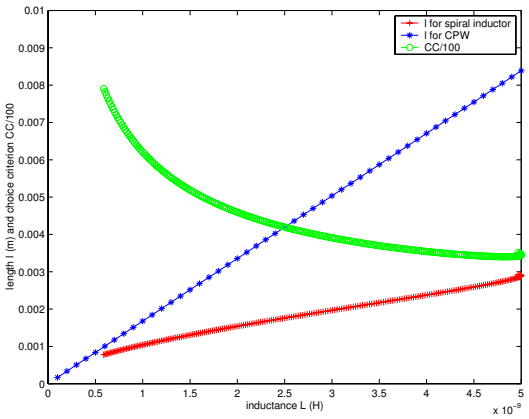

Figure 7. Inductor layout choice criterion

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