Influence of Back Ground Plane on New Radio Frequency Monochip Systems

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Abstract—**Every high frequency circuits need inductors for proper work. This is more and more true with new radio-frequency MOS transistors systems. But with the increase in frequency, lower inductors are required and MOS transistors offer less gain. Radio-frequency circuits in MOS technology are also obedient to the layout of low inductance high quality factor inductors. It has been shown that they can be better realized by microstrips. However, classical MOS digital technologies have no back ground plane under the substrate. This article analyzes the influence of parasitic back ground planes in the case of an often used coplanar solution : coplanar waveguide.**

Key Words: **coplanar waveguide, CPW, SOS**

1 Introduction

With the growth in the need for multimedia handled products, high frequencies and high bandwidth are now the real wagers for industry. However, this last cannot neglect low cost that is the main objective of its activities. That is why new research about radio-frequency (RF) structures on new CMOS digital technologies are nowadays done ([1],[2]). Indeed, traditional solutions for mixed-signal system on chip (SOC) such as flip chip attachment to package and embedded passives on it, fine pitch ball grid array or chip scale packaging are always linked to a higher cost than monochip projects. Thus since we cannot port digital part on GaAs or SiGe ICs that are classically used for high power and high frequency operations, the goal is to design the RF part on digital technologies. This also leads to lower cost since those last profit from the big consumption in computers. Studies on the RF front-end show immediately that the main point is the layout of inductors since they appear at every stage, from filter design to DC polarization, passing by resonator realization. Literature shows a lot of solutions for designing those inductors by minimizing lost into classical MOS substrate. But, new digital technologies rise up, which have properties between the MOS ones and the GaAs ones : Silicon-On-Insulator (SOI) and especially Silicon-On-Sapphire (SOS). Actually, in those case, substrate is a perfect insulator but MOS transistors are used and there is no ground plane under the substrate. Since it can be shown that a well suited way for layouting inductors is to use microstrips, the purpose of this paper is to study the influence of a back ground plane (parasitic or layouted) on the design of typical MMIC coplanar structure : coplanar waveguides (CPW). First classical method for computing CPW will be explained. Then the influence of back ground plane will be studied in different cases depending on the technological parameters. Finally, a practical discussion about design method and cares on an SOS technology will be processed as an example.

2 Coplanar waveguides calculus

It can be demonstrated that for small inductance, high Q inductors, the classical layout of fig. 1-(a) cannot be used at a reasonable cost in an industrial process ([3]). Analyzing an SOS $0.5\mu m$ technology, a method for choosing between classical printed spiral and CPW (fig. 1-(b)) is provided in [4] under the hypothesis that there is no ground plane under the sapphire substrate. However, those results must be discussed taking into account that when components are mounted on a board, there can be a back ground plane. Since it is demonstrated in those two quoted papers that the inductor value comes from the characteristic impedance Zc, we will focus on the study of this value. Wen ([5]) has shown in the last sixties that CPW where perfectly suitable for technologies which have no back ground plane and with high relative dielectric constant ϵ_r. He encouraged also integrated circuit designers to use this kind of line but it was forgotten mainly because electronic science broke into two separate domains : analog and RF. But with today issues, we must recall those advices and make a new study. The classical CPW structure is drawn on fig. 2 and we will use notations of this schematic for further work. According to [6], in case of a finite-substrate thickness, using the Schwartz-Christoffel conformal mapping (fig. 3), we need to solve (1).

$$W = F(\Phi, k) = \int_0^{\Phi} \frac{d\theta}{1 + k^2 sin^2\theta} \qquad (1)$$

Where $F(\Phi, k)$ is an incomplete elliptic integral of the first kind with amplitude Φ and modulus k. Then [7] gives us the quasi-static formula that leads to ϵ_{reff} and using the well known equation (2), we are now supposed to be able to calculate the influence of back ground plane on characteristic impedance of CPW.

$$Z_c = \frac{1}{C} * \frac{1}{c}\sqrt{\frac{1+\epsilon_r}{2}} \tag{2}$$

with ([6])

$$C = (1+\epsilon_r)\epsilon_0 \frac{2a}{b} \tag{3}$$

Results in [8] allow us to extend the previous method to the X band case. However, one must reminds that elliptic integrals are solve by numerical calculus ([9, 589-626]).
Other solutions for the calculus of the characteristic impedance of CPW mainly based on the optimization of the conformal mapping techniques can be found in the literature ([10], [11], [12]), but they are solved with numerical approximations. That is why the use of recent electromagnetic solvers should be taken into account. Its advantage is that it allows the computation of complex structure where conformal mapping often limits the study to one dielectric layer. We use *Momentum*© as 2.5 dimensions simulator with a dielectric defined by $\epsilon_r = 10.5$ in order to compute results given in fig. 4. They are the ϵ_{reff} values against the substrate thickness assuming the fact that the ground plane is just under the dielectric. The comparison between the simulated curve and the traditional one in the common area leads us to admit that simulator are as accurate as classical method (the maximum relative difference is 3%). However, the peak at about $1200\mu m$ proves that we must take care at the calculus method of the simulator : in this case, it seems that when the substrate thickness reach the wavelength in the dielectric a cyclical error appears. In the next part we will also simulate the dependence of the influence of the back ground plane on characteristic impedance on technological factors in the case of classical MOS technologies.

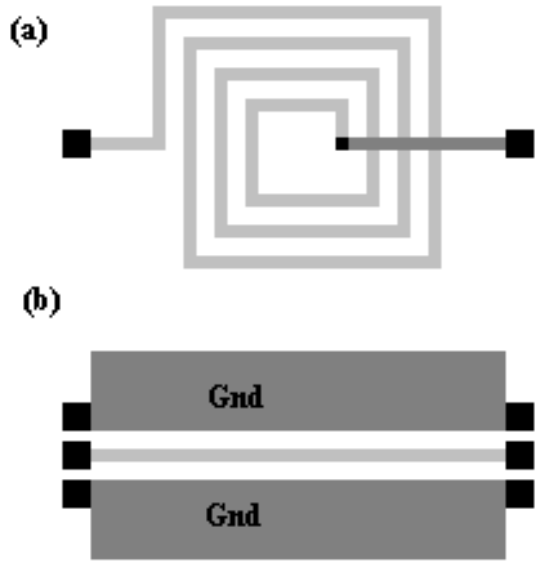

Fig.1: Inductors : (a)classical square spiral and (b)CPW

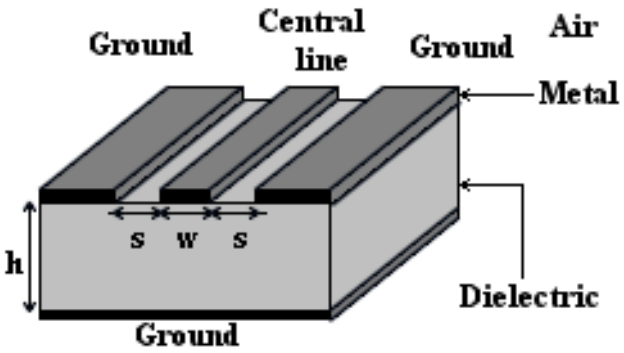

Fig.2: Coplanar waveguide (CPW)

3 Dependence of the influence of the back ground plane on characteristic impedance on technological factors

The peculiarity of MOS substrates is the fact that they are complex multilayer structures. However, if we assume that the influence of a parasitic ground plane can be too high for practical design, we can use metal layers other that the one of the CPW to create a shield. This results in the fact that there are only two interesting areas for our study. Actually, without attempting to the generality, we can assume that we have two dielectric layers and two metal layers. The top one is the one on which the CPW is layouted. The second one can be used as a shield. From fig. 4 we know that a specific study have to be done for some variations of the shield if it is closed to the CPW since the slope seems to be strong. Fig. 5 using the technological parameters given in table 1 sums up parameters of our simulations. We have focus our studies on the variation of the characteristic impedance against the distance of the ground plane to the CWP for different value of the relative dielectric constant of the substrate. We have chosen to simulate a CPW with Z_c of about 50Ω when there is no ground plane for a frequency of 10GHz. Thus we use $s = 50\mu m$ and $w = 115\mu m$. The simulator was *Momentum*© which we have been proven in the previous part to give faithful results and which have been validated concerning CPW cases in its documentation by comparison to [13].
Fig. 6 represents the results of the simulation of a shield layouted on the metal layer located in the area depict

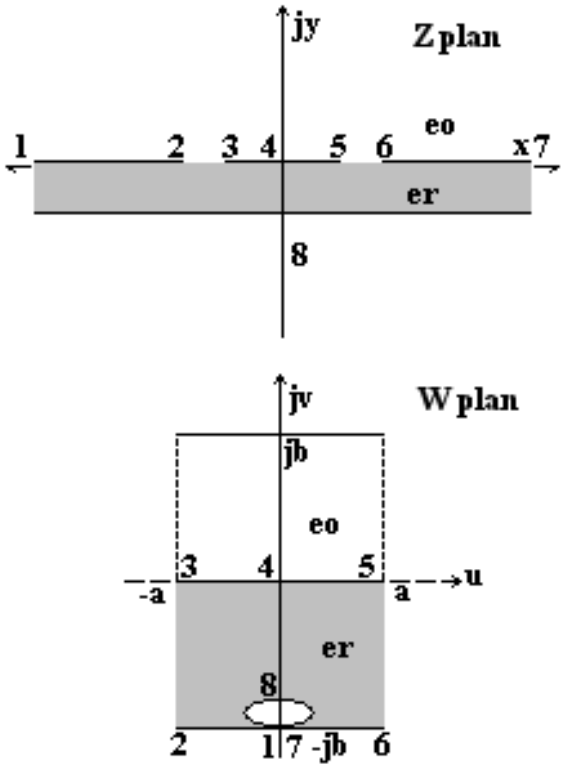

Fig.3: Conformal mapping structure

Table 1: Example of technology parameters

Thickness (μm)	Material	ϵ_r
∞	Air	1
CPW Metal Layer		
1.5	S_iO_2	3.9
Shield Metal Layer		
S_iO_2 thickness	S_iO_2	3.9
250	Dielectric	10 or 100
variable	Air	1
Parasitic Metal Layer		
∞	Air	1

by fig. 5-(a). Fig. 7 represents the results of the simulation of a parasitic grounded metal layer located in the area depict by fig. 5-(b). Results of the $\epsilon_r = 10$ case are given in the dot curves, and the one corresponding to $\epsilon_r = 100$ in the star curves. The first comment on those results is the fact that variations of the distance between the ground plane and the CPW either for far values or for closed ones lead to modification of the characteristic impedance. In order to well understand those curves, a practical case will be studied in the next section, without reducing the meaning of those results.

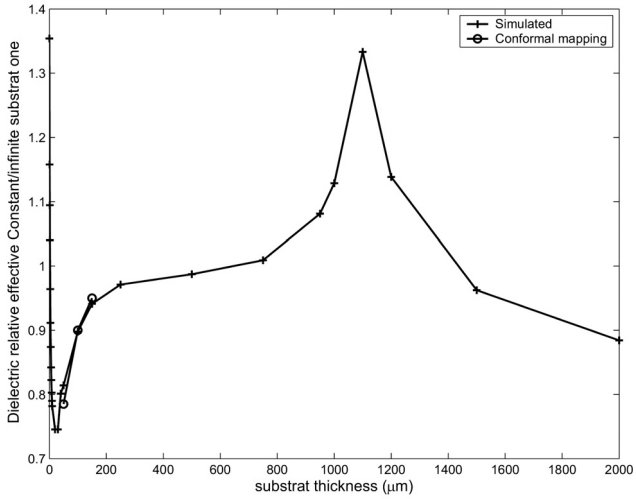

Fig.4: $\epsilon_{reff}/\epsilon_{reff_\infty}$ against substrate thickness

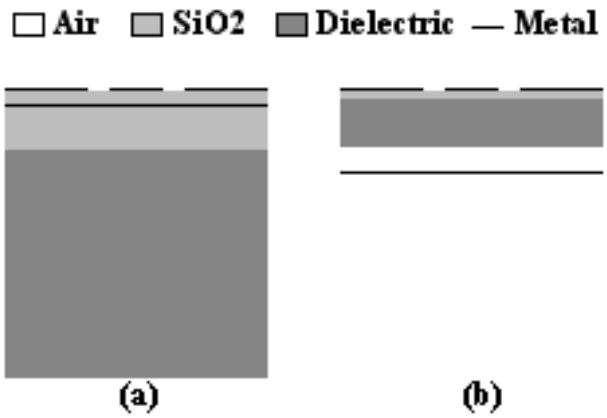

Fig.5: Area in which a ground plane can be. (a)As a shield on the second metal layer or (b)outside of the die

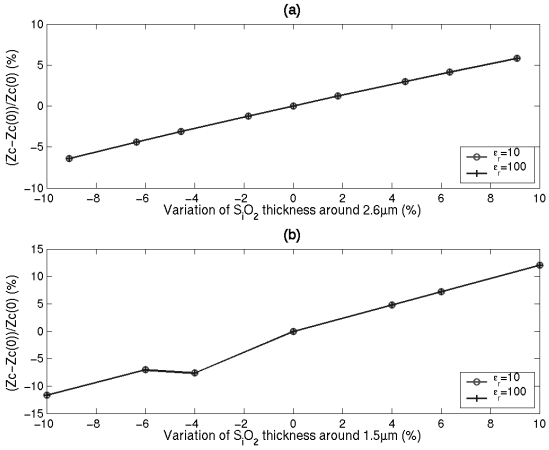

Fig.6: Variation of Z_c with the second metal layer position

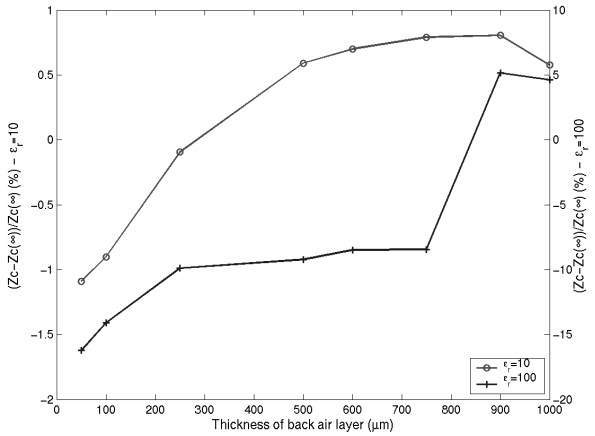

Fig.7: Variation of Z_c with the air substrate layer thickness

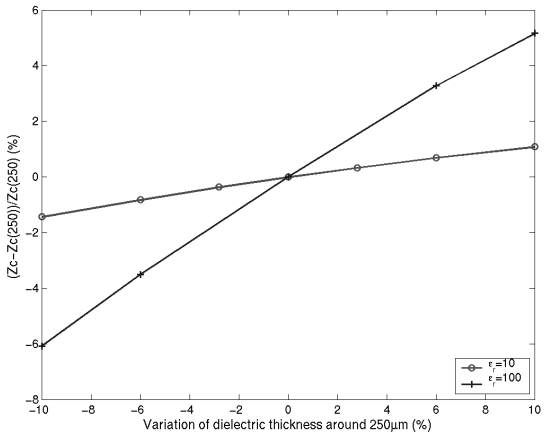

Fig.8: Variation of Z_c with the variation of the ground plane position just under the chip

4 Discussion about design method on an SOS technology and general care

Let us assume that we have an SOS technology. Sapphire dielectric constant is about 10 and so we can extract from the previous study a design method. The studied CPW has a $Z_{c\infty}$ of 45.158Ω. Fig. 7 shows that in the case of fig. 5-(b) if the air thickness is higher than twice the size of the one of the substrate, the relative variation of the characteristic impedance is less than 0.5%. However, if the ground plane is closed enough variation reaches and goes over 1%. With our technological parameters, this occurs for a distance smaller than 0.5mm, that can be considered as the thickness of the packaging box. We can consider that this error is higher than the one naturaly induced by process inaccuracies and thus it seems usefull to look for a shielding method.

The first one consists in using the solution previously exposed in fig. 5-(a). But, Fig. 6 agree with the first things we pointed out : when the distances reduce, the slope increase. Thus for a closed metal layer that could have been the first one, the position error is passed on with a factor of 65%. In the case of a closer metal, this factor can reach 120%. Those results do not depend on the relative constant of the dielectric material since the ground plane hide everything under it. Thus this shielding method cannot be used to hide a parasitic ground plane. Fig. 8 has been computed while assuming that there where a ground plane drawn just under the chip. It shows that the relative variation slope factor is of only 15% in the $\epsilon_r = 10$ case. This can be the wanted solution since it is the one that gives the most controled results.

Eventually, another solution in the field of technological research can be contemplated. Fig. 7 shows that the higher the relative dielectric constants the higher the influence of close ground plane is: this can be explained by (2) since the influence of the air layer ($\epsilon_r = 1$) on ϵ_{reff} grows with its thickness and the ratio of its relative dielectric value to the one of the substrate. Thus, for our peticular purpose, effort can be made on the design of MOS technologies on insulator substrates with low relative dielectric constant.

As a conlusion, we must point out the fact that the issue of the back ground plane is a general one that is not specific to analog designers, but can always appear when layouting coplanar lines. One must notice that with present conditions, GaAs designers are in the ideal case where a ground plane always exists under the substrate, but with mix between analog and hyperfrequency electronic fields, this peticularity has to be taken into account for every coplanar lines.

5 Conclusion

The study presented in this paper starts from the fact that analog designers now face radiofrequency problems that require hyperfrequency approach and method. Especially, the use of coplanar waveguide can be an important issue with novel MOS technologies that do not have control over the back ground plane. It have been shown that the position of an external parasitic plane has an influence on the characteristic impedance of the stripline that can be higher than the natural process variations. Two methods have been studied in order to hide its effect : the first one consists in layouting a plane and the second one in using low relative dielectric constant substrates. The first one turns out to be the easiest to realized but the only area in which the plane can be layouted is the one just under the package. The second one works out but needs technological research on substrate materials.

Acknowledgement

The authors gratefully acknowledge THALES Airborne Systems for funding the research.

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