

A Novel Approach for Radio Frequency Front End as Part of System-On-Chip in Digital MOS Technologies

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Abstract—This paper points out a classical optimum LNA structure and shows that its performances on a SOS $0.5\mu\text{m}$ digital technology at 10 GHz are poor compared with actual devices. However, while thinking in terms of global reception chain, a new factor of merit is computed and used, showing that those structures can be used in system-on-chip under certain assumptions.

Index Terms—LNA SOS FoM SOC

I. INTRODUCTION

The challenges in the area of radiofrequency (RF) and mixed-signal System-On-Chip (SOC) will become important as low-cost mobile and high bandwidth products derive across several market segments. The increasing performances of silicon ICs will enable lower cost solutions in the frequency domain below 10 GHz. GaAs ICs and SiGe ICs are now used for higher frequency or power applications. Signal integrity and cost issues become dominant. Considerations were made on flip chip attachment to package and embedded passives on this package. But the traditional solution of low inductance and high-density packages like fine pitch ball grid array (FBGA) or chip scale packaging (CSP) are always linked to a higher cost than mono-chip systems. The solution for the future is to use the same technology for both digital processing and analog part. This can only be done by parallelizing these two types of research. In the digital electronic and signal processing domain, higher speed analog to digital converters (ADC) are required, joined to harder data recovering algorithms. For analog people, the challenge is to find new RF structures in submicronic digital CMOS technologies or to generalize technology transpositions. The purpose of this work is to start such a study on the first block of the front-end : the low noise amplifier (LNA). First, classical and optimum LNA structures will be analysed in order to determine what kind of configuration should be transferred on digital technologies. Then LNA requirement will be computed from a global point of view, taking into account parameters of next stages. Indeed, philosophy of System-On-Chip is to consider the circuit as a global function with given features. Thus performances of elementary stages can disappear behind the fact that the chip succeeds in achieving specifications. Third, results that can be expected in Silicon-On-Sapphire (SOS) technology will be exposed, based on simulation of actual structures layouted in such technology. Finally a new Factor of Merit (FoM) will

TABLE I
CLASSICAL VALUES FOR MOS LNA

Author [Ref.]	NF (dB)	Gain (dB)	IIP_3 (dBm)	Power (mW)	f (GHz)
Shaeffer [6]	3.5	22	-9.5	30	1.5
Rafla [7]	2.5	22	-10	12	2.5
Floyd [8]	1.8	10	-2.8	8	0.9
Floyd [9]	1.2	14.5	-1	30	0.9
Rafla [10]	3	10	2	20	5.8
Sharaf [1]	3	12.2	-21	17	1
Gramegna [2]	1.75	10	3	27	0.9
Gramegna [3]	1.0	13	-1.5	8.6	0.92
Huang [11]	3	19.8	4.5	22.4	2.4
Yang [12]	2.2	15	1.3	7.2	2.4
Fouad [13]	2.74	21.6	-21.5	20.3	1
Tinella [4]	3	13.4	0	4.5	2.5
Floyd [5]	10	7.3	-7.8	79.5	26

be extracted so that performances of this work, a simulated 10GHz LNA, will be compared to recently produced structures. Extrapolation will be made and prediction of future performances will be concluded.

II. MOS LNA STATE OF ART

It appears when reading papers that some very finite rules governed LNA in high frequency. First of all is an analog global rule : low noise comes from few components. The preliminary intuitive structure could be reduced to only one active transistor. Then few structures can be derived from the first one (Fig. 1-(a)). We can lowered the noise by substituting resistance with self-inductance to obtain Fig. 1-(b). But stability problems appear and can generally be solved by isolating the drain-gate reverse path. The less noisy way to do it is to use the cascode schematic of Fig. 1-(c). Finally, since LNA are at the very beginning of the RF chain they should be 50Ω input-matched in order to be directly linked to the antenna without any other costly component. The input-impedance adaptation is usually done via an inductive source degeneration that also corresponds to the physical reality of packaging bond wire. Eventually, we obtain the classical structure of Fig. 1-(d) that is mostly used in RF front-ends (like [1], [2] and [3] on bulk CMOS or [4] and [5] on SOI - Silicon-On-Insulator). Table I shows typical performances in digital technologies (bulk or SOI) of variations around this optimum structure.

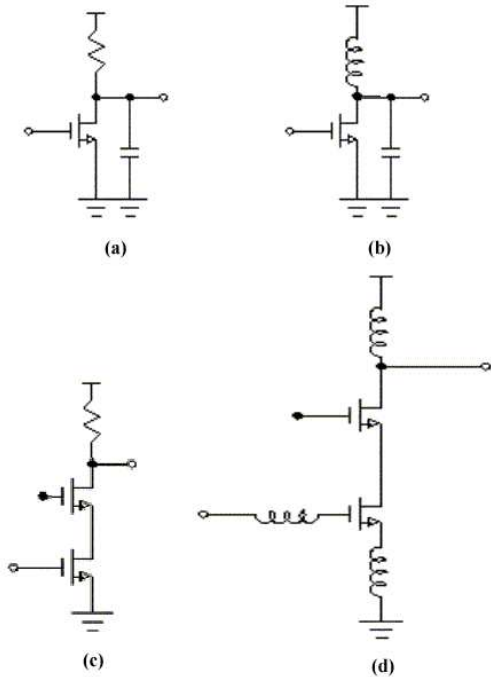


Fig. 1. Evolution of the LNA structure

III. REQUIRED PERFORMANCES OF LNA AS PART OF RECEPTION CHAIN

Even if the goal is to do the best LNA both in terms of gain and noise, a modest one can be excellent from a global point of view. Actually, what is really important for our purpose is to have a homogeneous chain both in the analog and the digital parts. Thus we can imagine that the simplest analog chain would be a LNA followed by a mixer that converts the RF signal to a base-band one. Then the ADC will complete the job. Let us assume our signal processor needs a 7dB maximum noise figure (NF) noted NF_{tot} which is a high but realistic value even in industry standard. Let us also assume that we can design a middle range mixer and a local oscillator, which implies that the mixer can be viewed as a two ports black box with a given NF_{mix} . Actually, every stage placed here can contribute to a global second stage equivalent noise figure called NF_2 . Then the LNA can be characterized by its gain and noise figure. For our purpose, since LNA only try to maximize the input impedance matching, we just have to take into account the gain that carries this information. By definition, the available gain (GA) is the most appropriated : it is the ratio between the available power at the output of the quadripole and the available power from the generator. This gain appears in the Friis formula ([14]) that gives :

$$F_{tot} = 1 + (F_{LNA} - 1) + \frac{F_2 - 1}{G_{LNA}^{lin}} \quad (1)$$

where F is the noise factor. All terms are numeric ratios and are not in decibel. Noise figure and gain in dB are given by $NF = 10\log(F)$ and $G = 10\log(G^{lin})$. For our purpose

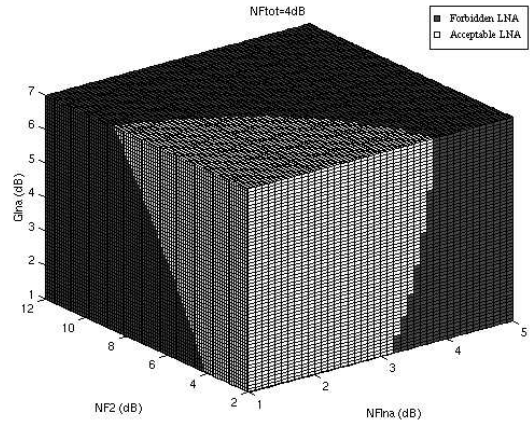


Fig. 2. Graphic resolution of equation (2)

we will use the inequality that can be derived from (1) where all the value are expressed in decibel :

$$10^{NF_{tot}/10} - (10^{NF_{LNA}/10} + \frac{10^{NF_2/10} - 1}{10^{G_{LNA}/10}}) \geq 0 \quad (2)$$

Thus we have one equation with three parameters which gives us a three dimensions space of solutions. While solving the problem we get the bright (that respects the global condition) and the dark (that does not) domains for the three parameters NF_2 , NF_{LNA} and G_{LNA} (Fig. 2).

IV. AN EXAMPLE OF SIMULATED LNA ON SOS

The structure pointed out in section II was simulated using SpectreRF on SOS $0.5\mu m$ technology. We have chosen to investigate this way first because from an analog point of view it has fewer parasitic capacitances and better inductors than classical bulk MOS or SOI technologies. Actually, passive components are better since there is no substrate. It is the case in our technology where inductors quality factors are about 10 up to 10 GHz thanks to a sapphire thickness of $250\mu m$. Then, from an industrial point of view, which is significant in SOC philosophy as said before, SOS is also considered as the next microprocessor substrate from the ITRS (International Technology Roadmap for Semiconductors). Thus we can plan for cost decrease of technologies that are now available and can already be used both for an analog use and a digital one. Practical design of our LNA will be part of another paper, but, as shown on table II computed from Fig. 3, 4, 5 and 6, results are worse than those of classical substrates (table I). Furthermore, they are poor compared to common standards. Nevertheless, according to Fig. 2, such LNA can be used in a reception chain under the hypothesis made before. Thus we have to introduce a new figure taking into account this new fact in order to make realistic comparisons and eventually define a roadmap.

V. LNA FIGURE OF MERIT

In this section we will define a new figure of merit included both LNA features and its impact in whole RF chain.

TABLE II
SOS 0.5 μm LNA SIMULATED PERFORMANCES

NF (dB)	Gain (dB)	IIP_3 (dBm)	Power (mW)	f (GHz)
3.53	5.16	5.55	12.42	10

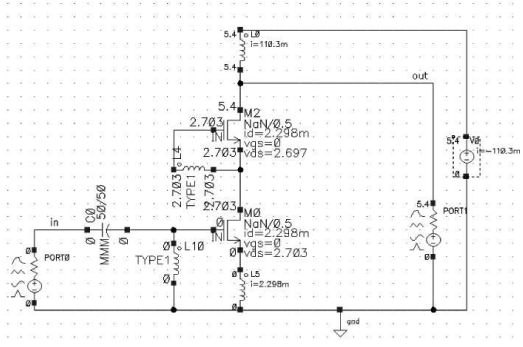


Fig. 3. Cascoded LNA in SOS0.5 μm

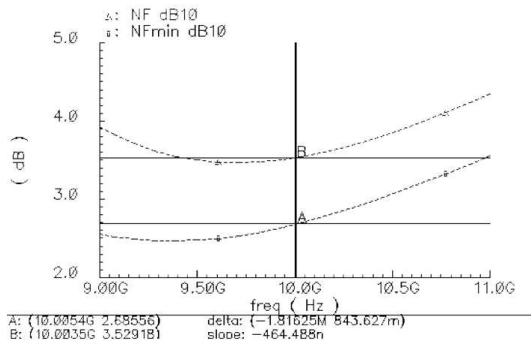


Fig. 4. Simulated noise figure and minimum NF

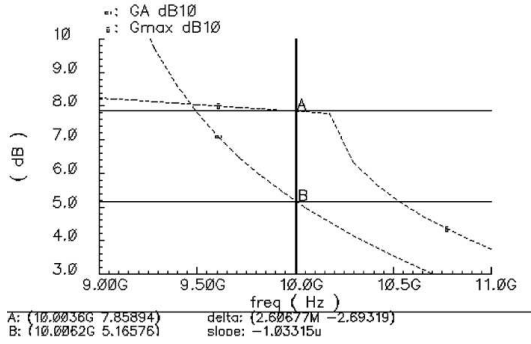


Fig. 5. Simulated gain and maximum gain

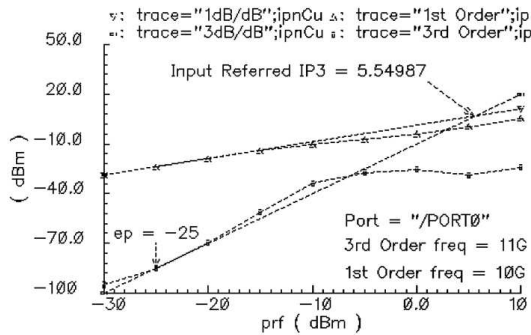


Fig. 6. Simulated IIP_3

Several features are listed below. First of all, as it is shown before, we can not neglect its gain and noise figure. The higher the gain is and the lower the NF is, the better is the LNA. Then of course is the frequency f . We did not speak about input referred third order intermodulation point (IIP_3) in previous sections. It is also an indicator of linearity and must be taken into account. But special attention is needed when remembering that IIP_3 can be negative. At the end, we will consider the value

$$|IIP_3|^{sgn(IIP_3)} \quad (3)$$

where $sgn(IIP_3) = IIP_3/|IIP_3|$ if $IIP_3 \neq 0$ and 0 otherwise. Eventually, further more in MOS technologies, the power consumption P is a negative indicator of merit. Here we get the classical FoM used by the SIA (Semiconductor Industry Association) excepted we use (3) instead of IIP_3 :

$$FoM_{SIA} = \frac{G \cdot IIP_3 \cdot f}{NF \cdot P} \quad (4)$$

But we need to introduce in our formula a new indicator of the performance of LNA inside the reception chain. First consider that the main goal of this first stage is to lower the noise figure of the chain. So our global indicator must be linked to noise. Fig. 2 gives us limits for G_{LNA} and NF_{LNA} for given NF_{tot} and NF_2 . Therefore, for a given NF_{tot} and NF_2 , the best LNA is the closest to the limit. Hence let us note Δ the distance between the optimum LNA and the actual one in the (NF_{LNA}, G_{LNA}) plane. We obtain eventually the following formula:

$$FoM_{LNA} = \frac{G \cdot |IIP_3|^{sgn(IIP_3)} \cdot f}{NF \cdot P} \frac{1}{\Delta + 1} \quad (5)$$

which gives the factor of merit of a LNA as part of a SOC. It shows the rightness of a LNA facing global system specifications and considering other blocks performances.

VI. PRESENT COMPARISONS AND ROADMAP

From all the structures presented here, we can build table III that gives FoM for actual LNA and simulated one. Let us compute it using a medium level system with $NF_{tot} = 7dB$ and $NF_2 = 9dB$. Fig. 7 is the graphical representation of the calculus of Δ , extracted from Fig. 2 looking at the plane $NF_2 = 9dB$. As a result, it appears that structures on SOS can be accurate enough for nowadays applications.

Moreover, it appears on Fig. 8 that such a classification using new FoM let us foresee a better evolution than the

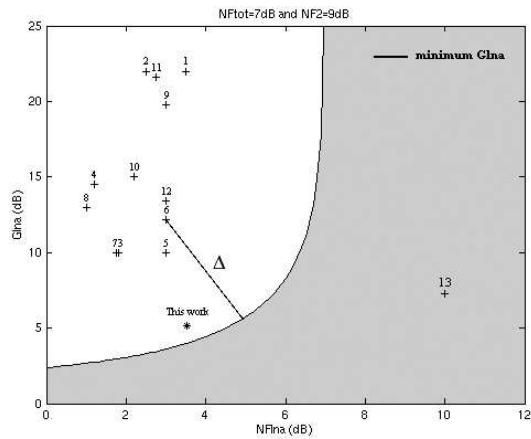


Fig. 7. LNA FoM calculus

TABLE III

FoM OF CLASSICAL LNA COMPARED TO THIS WORK

Number	Author [Ref.]	Year	Δ	FoM	Rank
1	Shaeffer [6]	1997	5.37	0.01	11
2	Rafla [7]	1999	6.05	0.03	10
3	Floyd [8]	1999	4.48	0.04	9
4	Floyd [9]	2000	5.61	0.05	8
5	Rafla [10]	2000	3.31	0.45	5
6	Sharaf [1]	2000	3.61	0.00	13
7	Gramegna [2]	2000	4.53	0.10	7
8	Gramegna [3]	2001	5.69	0.14	6
9	Huang [11]	2001	4.36	0.59	2
10	Yang [12]	2001	4.60	0.53	3
11	Fouad [13]	2001	5.61	0.00	12
12	Tinella [4]	2001	3.71	0.53	4
13	Floyd [5]	2002	Since work #13 falls into the dark side on Fig. 7, there is no factor of merit for [5]		
14	This work	2003	0.84	3.54	1

Moore's Law admits. Indeed, Moore's Law says that the channel length of MOS transistor must decrease by a factor $\sqrt{2}$ every 18 months. Now the transition frequency F_t of MOS devices can classically be written as a multiple of $1/L^2$ where L is the gate length. Thus using Moore's Law and equation (5), we can predict that the FoM progression will be quadrupled every 3 years. However the noise figure evolution does not decrease as fast as noise figure requirement dictated by digital progress. Now the NF_{tot} decreases by 3dB every times the bandwidth is doubled, assuming it is going to be every 3 years since it is the growth of data storage medium. Thus, including the LNA environment in the FoM allows to better appreciate the quality of LNA and its true weight in the reception chain. However, making the difference between "Actual FoM" and "Theoretical FoM" in Fig. 8 leads to an important error. It can be explained by the enhancement of inductors and devices. Inductors have two figure that characterize their performances : their quality factor and their resonant frequency. Also, frequency is already part of the figure of merit of inductors. Thus for a better comparison, let us avoid the use of the frequency in the FoM of LNA. This leads to the "(actual) FoM without frequency" curve that is better fitted by the "Theoretical FoM". Eventu-

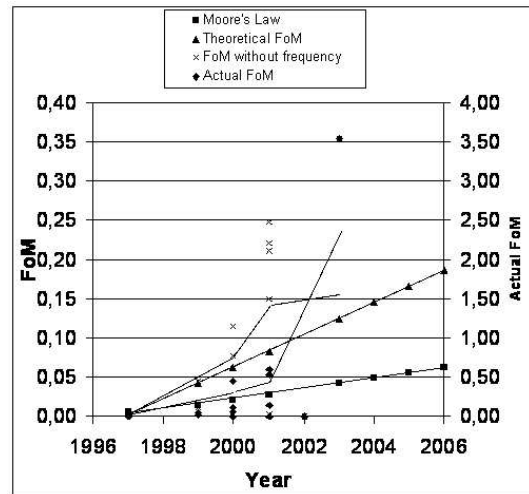


Fig. 8. LNA Roadmap

ally, Fig. 8 shows that our LNA, even with medium gain and NF, follows the predicted evolution. This result comes from the fact that our FoM takes care of multidomain research for a unique goal : the enhancement of the reception chain.

VII. CONCLUSION

Simulated results of cascoded LNA on a new digital SOS technology have been presented in this paper. They have been compared with current standard bulk MOS results from a conventional point of view. Therefore to better understand the real performance of a LNA, a new figure of merit is proposed to take into account its impact in the whole RF chain. This method of comparison gives encouraging results since it shows that we can progress faster than by just considering the Moore's Law. Thus the future of System on Chip lives in the concept of "system on substrate".

VIII. ACKNOWLEDGEMENT

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