A New Kind of CMOS High Frequency Oscillators

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***Abstract* — This paper presents a new 6.5GHz oscillator designed in a 0.5µm Silicon On Sapphire CMOS technology. This new structure is based on the principle of frequency multiplication integrated in the same stage than the generator. The layout particularities of it are presented in the case of a 8.5GHz fully integrated oscillator in the previous SOS technology that has an f_T of 35GHz. Given measurements results prove the functionality of our design.**

***Index Terms* — Analog integrated circuit, Microwave oscillators, MOSFET oscillators, Silicon on insulator technology.**

I. Introduction

Today, in our multimedia and mobile society, the importance of telecommunication is well known. Wireless communications systems, either the transmission path or the reception one, are build around the three key stages : amplifiers, mixers and frequency synthesizers. The latter is always based on a self oscillating system, the resonating frequency of witch is loop controlled. Those oscillators are the heart of frequency synthesizers and thus of receiver systems.

Moreover, industrial production requires low cost and, in the electronic field, this is linked to the use of digital technologies that have the advantages of mass production and use because of the increasing demand on computers and digital products. One of those widely used digital technology that could be utilized in order to design oscillators is the Silicon On Sapphire (SOS) one : it meets the costs requirements but must have less losses than classical CMOS since the substrate is here a true insulator. However , its main drawbacks is a lower frequency of transition (f_T) than other new CMOS technologies.

Also our goal in this paper will be to design a CMOS oscillator with the highest frequency that we can reached. In the first part, limits of the classical design method of oscillators in CMOS technologies will be pointed out and we will show that it cannot be used for the design of a 8.5GHz SOS oscillator. In the second part a new solution will be proposed, based on the use of non-linearities. In the third part, layouting issues and measurement results of this structure will be presented and finally discussion about its pros and cons will be performed.

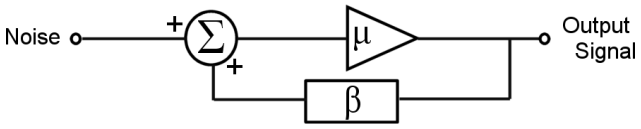

Fig. 1. A typical oscillator system.

II. CMOS RF Oscillator Design And Limits

An oscillator is a closed loop system that meets the Barkhausen's criteria. This kind of system can always be seen as the one of Fig.1. With its notation, Barkhausen's criteria are given by the following equations:

$$|H| \geq 1 \text{ and } \angle H = 0[2\pi] \quad (1)$$

With $H = \beta\mu$ the open loop transfer function.

In high frequency systems, the μ function is mostly realized through the use of one or more transistors and the β one through an LC tank. The controllability of such a system is given while having L or C that can be changed during operations. This leads to the classical oscillator designs like Hartley (Fig. 2-a) or Colpitts (Fig. 2-b) ones. But today differential output oscillators are required for better performances in the reception chain. Analysis and method of design are the same than for the previous ones and lead to the most widely used kind of oscillator in today's integrated circuits (ICs) shown in Fig. 2-c. In real ICs, efforts are mainly done on the design of the controllable part in order to have the largest available band without to much dependencies on parasitic effects. Anyway, the heart of frequency synthesizers is the one given in Fig. 2-c. An overview of today's performances of such a structure on CMOS technologies is given in Table I. We can see that it is difficult to reach a higher frequency of oscillations (f_0) than $f_T/10$, except in special cases like [1] in which we can use high Q hybrid technics because of the target frequency. In our case we want to design a 8.5GHz oscillator in a 0.5µm SOS technology with a f_T of 35GHz. The previous observations about Table I let us know that it will not be an easy challenge. More over, our simulations of the Fig. 2-c structure have shown that we actually cannot design a classical oscillator at a frequency

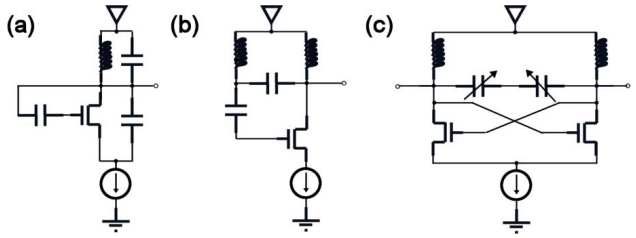

Fig. 2. Voltage Controlled Oscillator (VCO) topologies :

(a) Hartley, (b) Collpits and (c) Common differential one

higher than 6GHz which is about f_T/5.8. A new solution is thus needed and it will be the topic of the next part.

III. Classical Drawbacks Analysis And Novel Approach

The classical approach cannot be used to design an oscillator in CMOS technologies at a frequency higher than f_T /10. From a mathematical point of view, this is equivalent to the fact that Barkhausen's criteria cannot be met. Such a system is thus an amplifier or possibly an attenuator. In the case an amplifier cannot be designed in the chosen technology, two of the three essential blocks of the reception path presented in the introduction are missing, so there is no need to go further. On the other hand, let us assume that a selective amplifier at the desired frequency f_0 can be designed. In this case the only need is for an oscillator that can deliver harmonics or a way to generate those harmonics. Indeed, with such a system put together with the selective amplifier the required signal can be generated as it is shown in Fig. 3. The proposed solution uses a square wave generator called Abraham and Block multivibrator [5] as base stage, followed by a cascode amplifier in order to avoid parasitic return losses in the second stage [6] and to minimize the effects of the output load on the first stage conditions of oscillation.

The point in the presented solution is that the frequency multiplication results in the phase noise (PN) increase: actually, using the formula in the $1/f^2$ region given in [7],

$$PN(\Delta f) \approx 10\log\left[\frac{2FkT}{P_s}\left(\frac{f_0}{2Q\Delta f}\right)^2\right] \qquad (2)$$

the PN variation between the n^{th} and the m^{th} harmonics is:

$$\Delta PN_{m/n} \approx 20\log\left(\frac{m}{n}\right) \qquad (3)$$

TABLE I
Overview of CMOS Oscillator Performances

Author [Ref.]	Year	f_0	Technology	f_T
C. W. Wu [2]	2002	5GHz	CMOS 0.18µm	70GHz
Y. Park [3]	2004	4GHz	CMOS 0.25µm	65GHz
P. Andreani [4]	1999	2.4GHz	CMOS 0.80µm	20GHz

This results in a growth of a factor nine in the studied case, that is 19dB. However this decrease in performances of the oscillator could be compensated in two ways. First, since the base square oscillator is a low frequency one, its PN can be very low. Then, the PLL design will be simpler: indeed, the fundamental signal can be used instead of the output one. Thus a frequency divider can be removed what leads to less noise and losses. More over, with a multivibrator system that delivers a square signal, there is no more need for an analog to digital converter. The design of a complete integrated waves generator became suitable for a very low cost without a decrease in performances. Thus this paper will only focus on the feasibility of an oscillator without looking at its PN.

The schematic of Fig. 4 has been designed on a SOS 0.5µm technology. L_{pol} inductors are used to bias depleted NMOS. At first order, the frequency of oscillation is approximately given by (4).

$$f_0 \approx \frac{1}{2\ln 2 R_G C} \qquad (4)$$

The waveform is assumed to be perfectly square with a duty cycle of 1/2. R_D must be chosen high enough to deliver the correct bias current to the NMOS transistor and to be seen as an open circuit at high frequencies. The second stage is the classical cascode filter structure. C_{block} capacitors are used to filter the direct current but also combined with R_{IN} and L_{IN} make an impedance adaptation. In the same way L_{OUT} and C_{OUT} are both used as a bias and a 50Ω network.

In a second order approach, the influence of L_{pol} inductors must be taken into account. Thus L_{pol} have to be correctly chosen since they are in parallel with R_G and can modify oscillations. After having computed preliminary values, this circuit has been simulated. Results are given in fig. 5. It shows the spectrum density of the "square signal" generated by the first stage.

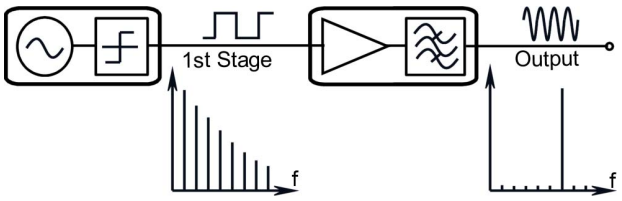

Fig. 3. Novel oscillator system design and principle.

IV. Layout Issues And Measurement results

In the SOS technology used, allows access to intrinsic NMOS transistors that result in the highest RF performances. In this case, the L_{IN} inductors of Fig. 4 are grounded at one end both from a DC and an AC point of view. Using the optimization under simulation for the matching of the second stage input filter (C_{block}, R_{IN}, L_{IN}), following values for the inductors have to be chosen: L_{IN}=350pH with Q=20. Since industrial requirements limit the usable die area because of costs and in order to avoid coupling with low frequency inductors L_{pol}, coplanar waveguides are used in order to layout L_{IN} following rules and results presented in [8].

This circuit is intended to be used in a total on-chip system packaging will not be used and it will be tested under probes. Thus, in order to have true measures a 50Ω match has been layouted on each port. With those practical constraints, the circuit was realized and the chip die photography is presented in Fig. 7. Measurements results are presented in Fig. 8.

They show that an oscillator at a central frequency of 6.5GHz in an 0.5µm SOS technology with a f_T of 35GHz can be designed and realized. This is an higher frequency than those obtain with the classical methods. However, results also show that the simulations do not allow to correctly predict the performances. Reasons why the quantitative performances have not been reached will be studied in the next part.

V. Discussion And Future Works

A. The amplitude issue

On some other circuits in this technology, for example amplifiers, differences between simulation and measurement results have been found. Our technology target is the 0 to 5GHz band and it seems that there is a second order pole at about 6GHz that does not appear in the model. Since we used a BSIM3v3 extracted model we are thinking that the saturation speed of electron is not well modelized for frequency above 5GHz. This can explain why the amplitude is so low but the validation of these theory will be part of future works on more simple structures. Anyway, the final actual amplitude is of the

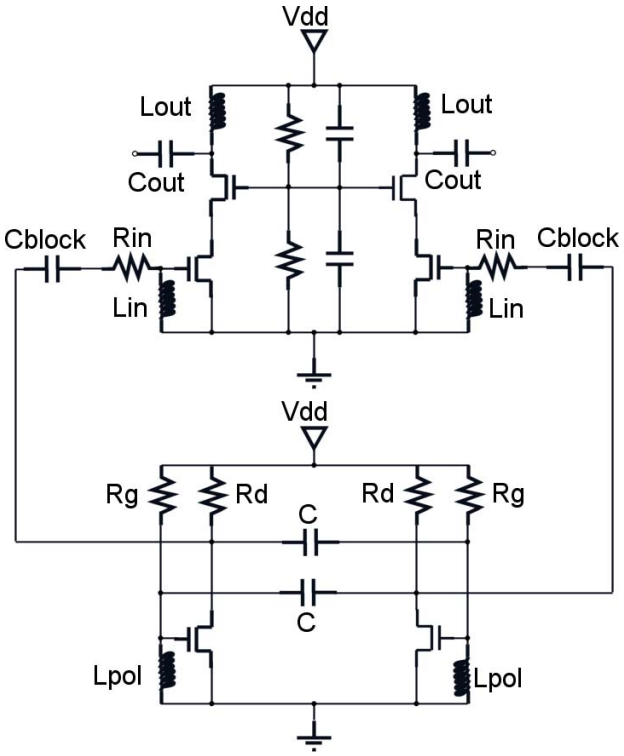

Fig. 4. A new kind of 8.5GHz MOS oscillator.

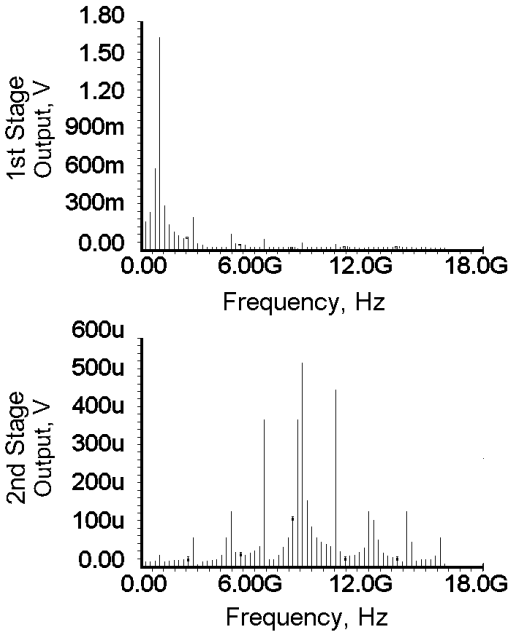

Fig. 5. Simulated frequency responses after the first and the second stage of Fig. 4 oscillator.

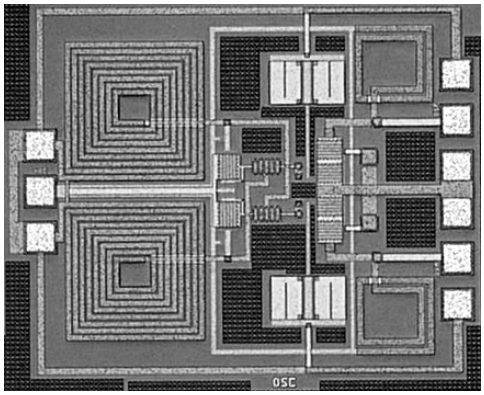

Fig. 6. Chip die photograph.

same order than the one shown in [1] what proves the usability of this structure.

B. The parasitic harmonics issue

In this case we know that it comes from lower quality factor Q of inductors than what it was assumed. This drawback inherent to silicon technology can be pointed out by reverse simulations. Also future works will have to focus on the design of cost-less (in term of occupied die area) and robust filters.

C. The central frequency shifting issue

This issue is clearly a mix between the two previous ones : indeed a too wide bandwidth for the filter and a low-pass effect in the amplifier with a cut-off frequency of 6GHz result in the selection of one of the inferior harmonics. This issue will also be removed automatically with the other two.

D. An other way of considering this solution

An other point of view of the presented new structure can be pointed out and should be investigated in future works. It consists in considering that the second stage is not only an amplifier but also a damped oscillator. It means that it has not enough gain in order to maintain the oscillations but, its response to a pulse generate damped oscillations. In this case, the coupled oscillator theory [9] can be applied and a look should be taken at it.

VI. Conclusion

In this paper a new kind of CMOS oscillator at 6.5GHz in a 0.5µm SOS technology has been presented. Classical design method of oscillators in CMOS technology has been studied and its limits shown. The main limit that was pointed out was a f_T of the technology too closed to the

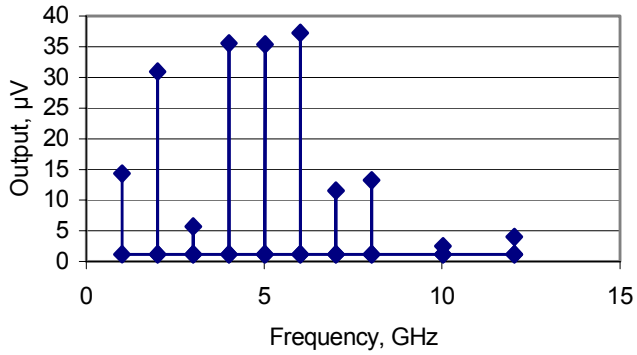

Fig. 7. Measured frequency responses at the output.

desired f_0. Thus a new kind of structure that avoids previous drawbacks has been proposed. It is based on the generation of a base signal full of harmonics and on the filtering of the desired one. The layout particularities of this new structure at 8.5GHz in a 35GHz f_T technology has been presented and results of measurements given. They show issues that have been pointed out but they prove the feasibility and the functionality of the oscillator. Finally, directions for future works for the improvement of models and quantitative performances have been given.

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